AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented) An integrated circuit (IC) comprising:

a processor core operable to perform data processing for the integrated circuit;

a cache memory operable to store data for the processor core; and

an on-chip memory operable to store data for the cache memory, wherein the cache memory is filled with data from the on-chip memory for cache misses, and wherein the on-chip memory is selectably filled with data from an external memory independent of cache accesses of the cache memory under user control.

2. (original) The integrated circuit of claim 1, further comprising:

a cache controller operable to handle memory transactions for the cache memory.

3. (original) The integrated circuit of claim 2, further comprising:

a direct memory exchange (DME) controller operable to handle data transfers between the on-chip memory and the external memory.

4. (original) The integrated circuit of claim 3, wherein the DME controller further operates with the cache controller to maintain data integrity for the cache memory.

5. (Previously Presented) The integrated circuit of claim 2, further comprising:

a direct memory access (DMA) controller operable to handle storage of DMA data received via at least one DMA channel to the cache memory or the on-chip memory, wherein the DMA controller further operates with the cache controller to maintain data integrity for the cache memory.

6. (cancelled)

7. (Previously Presented) The integrated circuit of claim 5, further comprising:

a direct memory exchange (DME) controller operable to handle data transfers between the on-chip memory and the external memory, wherein the DME controller couples to the DMA controller via at least one DMA channel.

8. (Previously Presented) The integrated circuit of claim 5, further comprising:

an internal memory bus coupling the on-chip memory, the cache controller, and the DMA controller, wherein the internal memory bus has a width that is equal to a line in the cache memory.

9. (cancelled)

10. (original) The integrated circuit of claim 1, wherein the cache memory and the on-chip memory are fabricated on same integrated circuit die.

11. (original) The integrated circuit of claim 1, wherein the cache memory and the on-chip memory are fabricated on different integrated circuit dies encapsulated within an IC package for the integrated circuit.

12. (Previously Presented) A wireless apparatus comprising:

an integrated circuit including

a processor core operable to perform data processing,

a cache memory operable to store data for the processor core, and

an on-chip memory operable to store data for the cache memory; and

an external memory operable to store data for the on-chip memory, wherein the cache memory is filled with data from the on-chip memory for cache misses, and wherein the on-chip memory is selectably filled with data from the external memory independent of cache accesses of the cache memory under user control.

13. (original) The integrated circuit of claim 12, further comprising:

a direct memory access (DMA) controller operable to handle storage of DMA data received via at least one DMA channel to the cache memory or the on-chip memory.

14. (Previously Presented) An integrated circuit comprising:

a first processor operable to perform general-purpose processing for the integrated circuit;

a second processor operable to perform data processing for the integrated circuit and including

a processor core operable to perform the data processing, and

a first cache memory operable to store data for the processor core;

an on-chip memory operable to store data for the first cache memory, wherein the first cache memory is filled with data from the on-chip memory for cache misses, and wherein the on-chip memory is selectably filled with data from an external memory independent of cache accesses of the first cache memory under user control; and

a first memory bus coupling the first and second processors to the external memory.

15. (Previously Presented) The integrated circuit of claim 14, wherein the second processor further includes a second cache memory operable to store instructions for the processor core, and wherein the second cache memory is automatically filled with instructions from the on-chip memory for cache misses.

16. (original) The integrated circuit of claim 15, wherein the second processor further includes

a first cache controller operable to handle memory transactions for the first cache memory,

a second cache controller operable to handle memory transactions for the second cache memory,

a direct memory access (DMA) controller operable to handle storage of DMA data received via at least one DMA channel to the first cache memory, the second cache memory, or the on-chip memory, and

a direct memory exchange (DME) controller operable to handle data transfers between the on-chip memory and the external memory.

17. (original) The integrated circuit of claim 16, wherein the DMA controller and the DME controller further operate with the first and second cache controllers to maintain data integrity for the first and second cache memories.

18. (Previously Presented) The integrated circuit of claim 16, wherein the second processor further includes a second memory bus coupling the on-chip memory, the first and second cache controllers, and the DMA controller, and wherein the DME controller couples to the DMA controller via at least one DMA channel.

19 - 34. (cancelled).

35. (Previously Presented) The integrated circuit of claim 3, wherein the DME controller is selectably programmable by the user to fill the on-chip memory with data from the external memory independent of the cache misses, to thereby provide the user control.

36. (Previously Presented) The integrated circuit of claim 35, further comprising:

a shared memory bus connected to the DME controller and the external memory; and

a direct memory access (DMA) controller coupled to the cache controller, an internal memory bus, and said shared memory bus, wherein said DMA controller has a plurality of DMA channels that can receive high-rate DMA data by way of the shared memory bus or the internal memory bus.

37. (Previously Presented) The integrated circuit of claim 36, wherein the DME controller couples to at least one of the plurality of DMA channels, and said DME controller is selectably programmable to fill the on-chip memory with data from the external memory by paging blocks of instructions or data.

38. (Previously Presented) The integrated circuit of claim 3, wherein the DME controller is selectably programmable by a user to schedule the filling of on-chip memory with data from the external memory.

39. (Previously Presented) The integrated circuit of claim 3, wherein the DME controller is selectably programmable by the user to control the filling of the on-chip memory with data blocks from the external memory such that the user functions as an anticipatory cache controller.

40. (Previously Presented) The integrated circuit of claim 3, wherein the DME controller is selectably programmable by the user to fill the on-chip memory with data from the external memory well in advance of need by the processor core and without paging-on-demand.

41. (Previously Presented) The integrated circuit of claim 1, wherein said integrated circuit is operable in a wireless device, said wireless device comprising:

an antenna to wirelessly communicate signals with a remote base station;

a receiver unit operably connected to said antenna and said integrated circuit to communicate a received signal from said antenna to said integrated circuit; and

a transmitter unit operably connected to said antenna and said integrated circuit to communicate data from said integrated circuit to said antenna as a transmission signal.

42. (Previously Presented) The integrated circuit of claim 1, wherein said integrated circuit is operable in a wireless device, said wireless device comprising:

means for communicating data between said integrated circuit and a remote base station.

43. (Previously Presented) The integrated circuit of claim 1, further comprising:

means for handling data transfers between the on-chip memory and the external memory, said means being selectably programmable by a user to fill the on-chip memory with data from the external memory independent of the cache misses.

44. (Previously Presented) The integrated circuit of claim 43, wherein said means is programmable to page blocks of instructions and/or data between the on-chip memory and the external memory.

45. (Previously Presented) The integrated circuit of claim 43, wherein said means is programmable to schedule the filling of the on-chip memory with data from the external memory.

46. (Previously Presented) The wireless apparatus of claim 12, further comprising:

a direct memory exchange (DME) controller operable to handle data transfers between the on-chip memory and the external memory.

47. (Previously Presented) The wireless apparatus of claim 12, further comprising:

a shared memory bus connected to the DME controller and the external memory; and

a direct memory access (DMA) controller coupled to a cache controller, an internal memory bus, and said shared memory bus, wherein said DMA controller has a plurality of DMA channels that can receive high-rate DMA data by way of the shared memory bus or the internal memory bus.

48. (Previously Presented) The wireless apparatus of claim 46, wherein said DME controller couples to at least one of a plurality of DMA channels, and said DME controller is selectably programmable to fill the on-chip memory with data from the external memory by paging blocks of instructions or data.

49. (Previously Presented) The wireless apparatus of claim 12, wherein the DME controller is selectably programmable by a user to schedule the filling of on-chip memory with data from the external memory.

50. (Previously Presented) The wireless apparatus of claim 12, further comprising:

an antenna to wirelessly communicate signals with a remote base station;

a receiver unit operably connected to said antenna and said integrated circuit to communicate a received signal from said antenna to said integrated circuit; and

a transmitter unit operably connected to said antenna and said integrated circuit to communicate data from said integrated circuit to said antenna as a transmission signal.

51. (Previously Presented) The wireless apparatus of claim 12, further comprising:

means for communicating data between said integrated circuit and a remote base station.

52. (Previously Presented) The wireless apparatus of claim 12, further comprising:

means for handling data transfers between the on-chip memory and the external memory, said means being selectably programmable by a user to fill the on-chip memory with data from the external memory independent of the cache misses.

53. (Previously Presented) The wireless apparatus of claim 52, wherein said means is programmable to page blocks of instructions and/or data between the on-chip memory and the external memory.

54. (Previously Presented) The wireless apparatus of claim 52, wherein said means is programmable to schedule the filling of the on-chip memory with data from the external memory.